REMARKS

In view of the above amendment and the following discussion, the Applicants submit that none of the claims now pending in the application are made obvious under the provisions of 35 U.S.C. § 103. Thus, the Applicants believe that all of these claims are now in allowable form.

I. REJECTION OF CLAIMS 1-15 U.S.C. § 103

A. Claims 1-14

The Examiner has rejected claims 1-14 in the Office Action under 35 U.S.C. § 103 as being unpatentable over Chong, et al. (US Patent 6,624,489, issued September 23, 2003, hereinafter referred to as "Chong".) in view of Buynoski, et al. (US Patent 6,518,113, issued February 11, 2003, hereinafter referred to as "Buynoski"). The Applicants respectfully traverse the rejection.

Chong teaches formation of silicided shallow junctions using implant through metal technology and laser annealing process. The method taught by Chong forms a gate transistor comprising a silicide layer, heavily doped layer, polysilicon layer and a gate oxide layer, in that order. (See Chong, Fig. 11, Col. 5, Line 44 - Col. 6, Line 15.)

Buynoski teaches doping of thin amorphous silicon work function control layers of MOS gate electrodes. Buynoski's method applies to in-laid ("damascene") gates. (See Buynoski, Col. 1, Lines13-15.) Both methods taught by Buynoski involve forming the source drain regions, forming a doped polysilicon layer over a thin gate insulator layer and then filling a void with a metal contact (i.e. the "damascene" method). (See Buynoski, Fig. 7(A), Fig. 16(A); Col. 12, Line 43 - Col. 13, Line 21.)

The Examiner's attention is directed to the fact that Chong and Buynoski, individually or in any permissible combination, fail to teach, show or suggest the Applicants' invention. Chong and Buynoski fail to teach, show or suggest the novel method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor that includes the step of siliciding the polysilicon gate electrode to form a silicide adjacent to said gate dielectric layer, as positively claimed by the Applicants' independent claim 1. Specifically, Applicants' independent claim 1 positively recites:

1. A method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor, comprising the steps of:

(a) providing a substrate;

(b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer of a gate structure of the transistor;

(c) doping the polysilicon layer using at least one dopant;

(d) forming a polysilicon gate electrode of the gate structure;

(e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and

(f) siliciding the polysilicon gate electrode to form a silicide adjacent to said gate dielectric layer. (Emphasis added.)

The Applicants' invention teaches a novel method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor that includes the step of siliciding the polysilicon gate electrode to form a silicide **adjacent** to said gate dielectric layer. Utilizing the Applicants' inventive method leads to improved work function and electron mobility. (See Applicants' Specification, Page 8, Paragraph [0028], and Fig. 3.)

The Examiner's attention is directed to the fact that Chong and Buynoski, alone or in any permissible combination, fail to teach, show or suggest the Applicants' invention. Chong teaches a transistor that comprises of the following sequence of layers: a silicide layer, heavily doped layer, polysilicon layer and a gate oxide layer. (See Chong, Fig. 11, Col. 5, Line 44 - Col. 6, Line 15.) Note that the silicide layer **is not adjacent to** the gate oxide or gate dielectric layer. Furthermore, Buynoski teaches a transistor that comprises of the following sequence of layers: a metal gate layer, doped polysilicon layer, and a thin gate insulator layer. (See Buynoski, Fig. 7(A), Fig. 16(A); Col. 12, Line 43 - Col. 13, Line 21.) Again, note that the silicide layer **is not adjacent to** the gate oxide or gate dielectric layer. In fact, Buynoski does not even teach having a silicide gate, but rather a metal gate. In contrast, Applicants' independent claim 1 positively claims a step of siliciding the polysilicon gate electrode to form a silicide **adjacent** to said gate dielectric layer.

In addition, the Applicants respectfully submit that Chong and Buynoski cannot be meaningfully combined. Chong teaches a method of creating a gate transistor from annealing polysicilicon with a metal cap. Buynoski teaches creating a metal gate transistor from a "damascene" process by filling a void with a metal layer. These two methods are completely independent of each other and have different problems that are

not present in the other method. For example, the "damascene" method taught by Buynoski may have metal adhesion issues or voids in the metal layer causing shorts that may not be an issue in the method taught by Chong. As such, the Applicants respectfully submit that Chong and Buynoski cannot be meaningfully combined.

In arguendo, even if Chong and Buynoski were combined, the combination would still not teach or suggest Applicants' invention. The combination of Chong and Buynoski would only teach a method of forming a transistor comprising layers in the following sequence: a silicide layer, a heavily doped polysilicon layer, a polysilicon layer, a doped polysilicon layer and a gate oxide. Therefore, the combination of Chong and Buynoski does not teach or suggest Applicants' invention as recited in independent claim 1.

Dependent claims 2-14 depend, either directly or indirectly, from claim 1 and recite additional limitations. As such, and for the exact same reason set forth above, the Applicants submit that claims 2-14 are also not made obvious by the teachings of Chong and Buynoski. As such, the Applicants respectfully request the rejection be withdrawn.

B. Claim 15

The Examiner has rejected claim 15 in the Office Action under 35 U.S.C. § 103 as being unpatentable over Chong, et al. (US Patent 6,624,489, issued September 23, 2003) in view of Buynoski, et al. (US Patent 6,518,113, issued February 11, 2003) and further in view of Vaidya et al. (Effect of Dopant Implantation on the properties of $TaSi_2$/poly-Si composites). The Applicants respectfully traverse the rejection.

Vaidya discloses the effect of dopant implantation and redistribution on the properties of $TaSi_2$/poly-Si structures.

The Examiner's attention is again directed to the fact that the alleged combination fails to teach the step of siliciding the polysilicon gate electrode to form a silicide **adjacent** to said gate dielectric layer. Namely, the substantial gap left by Chong and Buynoski is not bridged by Vaidya. Specifically, Vaidya also fails to disclose the concept of siliciding the polysilicon gate electrode to form a silicide **adjacent** to said

gate dielectric layer. As such, the combination of Chong and Buynoski with Vaidya would not make Applicants' claim 15 obvious.

Dependent claim 15 depends from claim 1 and recites additional limitations. As such, and for the exact same reason set forth above, the Applicants submit that claim 15 is also not made obvious by the teachings of Chong, Buynoski and Vaidya. As such, the Applicants respectfully request the rejection be withdrawn.

Conclusion

Thus, the Applicants submit that all of these claims now fully satisfy the requirement of 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the issuance of a final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Kin-Wah Tong, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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